IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|---|
| Applicant | : Kiyoshi Kato | Art Unit : | 2825 |
| Serial No. | : 10/595,567 | Examiner : | Magid Y Dimyan |
| Filed | : April 27, 2006 | Confirmation No.: | 2837 |
| | | Notice of Allowance Date: November 13, 2008 | |
| Title | : SEMICONDUCTOR INTEGRATED CIRCUIT AND DESIGN METHOD THEREOF | | |

**MAIL STOP ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance mailed November 13, 2008, enclosed is a completed issue fee transmittal form PTOL-85b. The amount of $1,810 for the required issue and publication fees is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any additional charges or credits to our Deposit Account No. 06-1050.

Respectfully submitted,

Date: February 12, 2009

Hussein Akhavannik
Reg. No. 59,347

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